Instruction-level Parallelism (ilp)

In a single processor, MLP may be considered a form of instruction-level parallelism (ILP). However, ILP is often conflated with superscalar, the ability to execute conditional instructions constructs. Recent innovations in memory system and scheduling techniques required support for instruction-level parallelism (ILP).

Watch on Udacity: udacity.com/course/viewer#!/c-ud007/l-3615429333/m.

CiteSeerX - Document Details (Isaac Councill, Lee Giles, Pradeep Teregowda): Wide issue superscalar and VLIW processors utilize instruction-level parallelism. Abbreviated as ILP, Instruction-Level Parallelism is a measurement of the number of operations that can be performed simultaneously in a computer program. The 90s: Instruction-Level Parallelism. – Superscalar out-of-order processors, cache hierarchies. – Low-cost desktops, supercomputers. • The 2000s: Multicore.

Eg vector/SIMD instruction set extensions (SSE, AVX etc). What are the fundamental limits to how much instruction-level parallelism can be extracted. Pipeline increases the throughput by improving instruction level parallelism (ILP). Instruction level parallelism: the processor can perform. More Than Just Megahertz, Pipelining & Instruction-Level Parallelism, Deeper Pipelines – Superpipelining, Multiple Issue – Superscalar, Explicit Parallelism – architectures, microprocessor pipelining, instruction-level parallelism, data-level parallelism, thread-level parallelism, and request-level parallelism.

Prerequisite: Instruction-level parallelism (ILP) is a measure of how many of the operations in a computer program can be performed simultaneously. The potential overlap cannot continue to leverage Instruction-Level parallelism (ILP). Single processor performance improvement ended in 2003. New models for performance: Instruction-level Parallelism (ILP). ILP has as its objective the execution in parallel of the lowest level machine operations, such as memory loads and stores.

Matthew A. Postiff, David A. Greene, Gary S. Tyson, Trevor N. Mudge, The limits of instruction level parallelism in SPEC95 applications, ACM SIGARCH.

A good explanation on Instruction Level Parallelism (ILP) can be found at CUDA Performance: Maximizing Instruction-Level Parallelism. It has been pointed out...

Summary: ILP dates backs to the 1940s, and various attempts have been made.


Keywords: Chip Multiprocessor (CMP), Data Level Parallelism (DLP), Thread Level Parallelism (TLP), Instruction Level Parallelism (ILP), Memory Level Extraction of Massive Instruction Level Parallelism. Augustus K. Uht. Dept. of Electrical Engineering. Kelley Hall. Univ. of Rhode Island. Kingston, RI 02881, USA.

But I can't find any references for ILP in the documentation or the architecture white papers. As far as I can see, each CUDA core (or SIMD lane) has integer.

CPE 731 Advanced Computer Architecture Instruction Level Parallelism Part I. Dr. Gheith Abandah. Adapted from the slides of Prof. David Patterson, University. Say you have an ISA where all instructions are 32-bits and which has 16 general _X_ The pipeline is able to better exploit instruction level parallelism.